We Claim:

1. An integrated, tunable capacitance device, comprising:

a semiconductor body being of a first conductivity type and having a semiconductor region with a terminal region for applying a tuning voltage;

at least one first insulating region being introduced into said semiconductor body and having a first layer thickness;

a second insulating region applied to said semiconductor body adjoining said at least one first insulating region and having a common interface with said semiconductor region, said second insulating region having a second layer thickness less than said first layer thickness;

a gate electrode on said second insulating region, said semiconductor region having a partial region disposed below said gate electrode, said at least one first insulating region being disposed between said terminal region and said partial region; and

a region being introduced into said semiconductor body for connection to a reference-ground potential, said region adjoining said semiconductor region, being of a second conductivity type, and being highly doped.

2. The capacitance device according to claim 1, wherein said gate electrode completely covers said second insulating region and partly covers said first insulating region.

3. The capacitance device according to claim 1, wherein said gate electrode has a periphery and adjoins said at least one first insulating region along said periphery.

4. The capacitance device according to claim 1, wherein:

said semiconductor region is of said first conductivity type and is formed as a well; and

said terminal region is formed as a well terminal region of said first conductivity type having a dopant concentration higher than a doping concentration of said semiconductor region.

5. The capacitance device according to claim 4, further comprising a second region of said first conductivity type, said second region:

being connected to said semiconductor region;

having a doping concentration higher than said semiconductor region; and

being connected to said well terminal region.

6. The capacitance device according to claim 1, wherein said gate electrode is formed from a polycrystalline layer.

7. The capacitance device according to claim 1, wherein said gate electrode is a polycrystalline layer.

8. The capacitance device according to claim 1, wherein said first insulating region is an oxide region.

9. The capacitance device according to claim 8, wherein said first insulating region is a shallow trench insulation region.

10. The capacitance device according to claim 9, wherein said second insulating region is an oxide region.

11. The capacitance device according to claim 1, wherein said second insulating region is an oxide region.

12. An integrated, tunable capacitance device, comprising:

a semiconductor body being of a first conductivity type and having a semiconductor region with a terminal region for applying a tuning voltage;

at least one first insulating region being introduced into said semiconductor body and having a first layer thickness;

a second insulating region applied to said semiconductor body adjoining said at least one first insulating region and having a common interface with said semiconductor region, said second insulating region having a second layer thickness less than said first layer thickness;

a gate electrode on said second insulating region, said semiconductor region having a partial region disposed below said gate electrode, said at least one first insulating region being disposed between said terminal region and said partial region; and

a region being introduced into said semiconductor body for connection to a reference-ground potential, said region adjoining said semiconductor region, being of a second conductivity type, and having a doping concentration higher than a doping concentration of said semiconductor body.

13. An integrated, tunable capacitance device, comprising:

a semiconductor body being of a first conductivity type and having:

a semiconductor region having a terminal region for applying a tuning voltage; and

at least one first insulating region having a first layer thickness;

a second insulating region at said semiconductor body adjoining said at least one first insulating region and having a common interface with said semiconductor region, said second insulating region having a second layer thickness less than said first layer thickness;

a gate electrode at said second insulating region, said semiconductor region having a partial region disposed below said gate electrode, said at least one first insulating region being disposed between said terminal region and said partial region; and

a region being introduced into said semiconductor body for connection to a reference-ground potential, said region adjoining said semiconductor region, being of a second conductivity type, and having a doping concentration higher than a doping concentration of said semiconductor body.

14. The capacitance device according to claim 13, wherein said gate electrode completely covers said second insulating region and partly covers said first insulating region.

15. The capacitance device according to claim 13, wherein said gate electrode has a periphery and adjoins said at least one first insulating region along said periphery.

16. The capacitance device according to claim 13, wherein:

said semiconductor region is of said first conductivity type and is formed as a well; and

said terminal region is formed as a well terminal region of said first conductivity type having a dopant concentration higher than a doping concentration of said semiconductor region.

17. The capacitance device according to claim 16, further comprising a second region of said first conductivity type, said second region:

being connected to said semiconductor region;

having a doping concentration higher than said semiconductor region; and

being connected to said well terminal region.

18. The capacitance device according to claim 13, wherein said gate electrode is formed from a polycrystalline layer.

19. The capacitance device according to claim 13, wherein said gate electrode is a polycrystalline layer.

20. The capacitance device according to claim 13, wherein said first insulating region is an oxide region.

21. The capacitance device according to claim 20, wherein said first insulating region is a shallow trench insulation region.

22. The capacitance device according to claim 21, wherein said second insulating region is an oxide region.

23. The capacitance device according to claim 13, wherein said second insulating region is an oxide region.